



2025 SEE/MAPLD Workshop Call for Papers

May 12 – 16, 2025
San Diego Marriott La Jolla, La Jolla, CA

Please join us for 2025 Single Event Effects (SEE) Symposium and Military and Aerospace Programmable Logic Devices (MAPLD) Workshop to be held jointly May 12-16, 2025 in La Jolla, California.

We are seeking contributions in the areas below, but all submissions will be reviewed. Four sessions are available: **SEE, MAPLD, Combined and Poster**. The Combined Session includes submissions that cross SEE and MAPLD themes. The Poster Session can include SEE, MAPLD, or Combined content. Please refrain from technical content reasonably classified as product marketing. Paper submissions are due on **February 21, 2025**.

We especially encourage submissions focusing on, but not limited to:

- Standards and methods (new or adapted)
- Heavy-ion, proton, and alternative SEE testing
- Test facility updates
- Space environments
- Modeling and Simulation approaches (new or adapted)
- Applications of AI/ML to SEE testing, analysis, and mitigation
- Mission applications and highlights enabled by FPGAs/SoCs
- Device failure modes and reliability
- Reconfigurable High-Performance Computing, evolvable hardware and security
- NextGen Platforms and Sensors Enabled by FPGAs/SoCs
- Tool Enablement

Abstract Submission Guidelines:

- Formats: Word (.docx), PowerPoint (.pptx), or (.pdf) only.
 - Word or PDF: 1-4 pages maximum.
 - PowerPoint: Title page with authors and affiliations, motivation/context/overview, available relevant results, and anticipated conclusions.
- Utilize templates available on our website.
- Submit online (<https://www.seemapld.org/>) before the deadline.

Submission Deadline: February 21, 2025

The conference committee will notify all prospective speakers of acceptance status by March 21, 2025.

SEE Symposium / Combined* / MAPLD Session Options

<p>Single-Event Phenomena, Mechanisms & Modeling: Upsets, Functional Interrupts, Transients, Latchup, Gate Rupture, Burnout, etc. Destructive and Non-Destructive Effects, Nanoscale Phenomena, Charge Transport and Collection, Impact of Circuit and Environmental Parameters, etc.</p>	<p>FPGAs/SoCs, PLDs, New Devices, and Design: Novel FPGA and PLDs; Benchmarking; Applications of space-borne processing. Agile methods, ESL/HLS and model-based engineering techniques, embedded processing, and synthesis efficiency improvements.</p>
<p>SEE Mitigation: Device Level SEE Mitigation Methods including Radiation Hardened by Design (RHBD) and by Process (RHBP): Approaches for gaining SEE hardness in commercial devices, etc.</p>	<p>SEE Mitigation: Circuit and System Level Multi-level approaches for high reliability and fault tolerance (RHBD, redundancy, TMR, SET filtering, etc.), upset mitigation techniques, automated tools, etc.</p>
<p>Environments and Facilities: Space, Atmospheric, and Terrestrial environments. Heavy-Ion, Proton, Neutron, Pulsed Laser and Other Test Facilities. Correlation between environment and test.</p>	<p>Validation and Verification: Techniques and languages such as co-simulation, System Verilog and OVM/UVM, etc. Simulation, emulation, new tools and methods for design validation.</p>
<p>Device Data and Measurement: Techniques for Memories, Analog/Digital Circuits, Systems-on-Chip (SoCs), FPGAs, Optocouplers, Photonic ICs, Power Converters, Sensors, etc.</p>	<p>Availability, Reliability, and Susceptibility: Failure mechanisms, reliability testing and characterization, packaging reliability, reliable design practices.</p>
<p>Case Study: Devices and Systems Operational Regimes and Performance Data for Systems and Devices from LEO to Interplanetary, High Altitude Aircraft, and Terrestrial.</p>	<p>Case Study: Computing, Logic, and Processing Novel applications of Reconfigurable computing, high-performance processing and successful deployment of programmable logic, etc.</p>
<p>Systems and Error Rate Computation: Error Mitigation, EDAC, Multi-core Processing, and Fault Tolerant Systems; Analytic, Monte Carlo, Mixed-Level, methods, etc.</p>	<p>Research and Education: Education Practices, Market Demands, and Retention. Training course overview and organization, Degree programs, Relevant future trainings 2024.</p>
<p>Artificial Intelligence (AI) / Machine Learning (ML) in FPGAs/SoCs: AI / ML design considerations for reliable terrestrial, avionic, and aerospace applications; using AI for SEE mitigation; SEE evaluation of designs leveraging AI / ML</p>	
<p>*All options subject to change any time, per the discretion of the conference committee</p>	

2025 Conference Committee

Krysten Pfau, Lockheed Martin, SEE General Chair

Michael Wirthlin, BYU, MAPLD Chair

Justin Likar, JHU/APL, SEE Technical Chair

Michael McKenna, Missile Defense Agency; **Ken LaBel**, NASA (ret.), Tutorial Chairs

Martha O'Bryan, SSAI / GSFC, Poster Session Chair

Larissa Milic, EMPC, Exhibit Chair

Teresa Farris, Archon, LLC, Meeting Planner

Carl Szabo, SSAI / GSFC, AV Chair